

Claims

- [c1] 1. A method of forming a floating gate, comprising:
- providing a substrate having at least a device isolation structure, an active region defined by the device isolation structure, a pad layer formed over the active region, a mask layer formed over the pad layer, and a trench formed in the substrate, wherein the trench penetrates through the pad layer and the mask layer;
 - forming a tunnel oxide layer on a surface of the trench;
 - forming a conductive layer in the trench;
 - removing a portion of the conductive layer by an isotropic etching process, wherein a top surface of a remaining conductive layer is concave;
 - etching the remaining conductive layer until a portion of the tunnel oxide layer is exposed by an anisotropic etching process, wherein byproduct polymer residues are generated and serve as a mask during the anisotropic etching process; and
 - removing the byproduct polymer residues, the mask layer and the pad layer so as to form a first floating gate and a second floating gate having sharp top-corners over a plurality of sidewalls of the trench.

- [c2] 2 The method of claim 1, wherein the isotropic etching process comprises a wet etching process.
- [c3] 3. The method of claim 2, wherein the wet etching process is performed by using a solution consisting of ammonia water, hydrogen peroxide and deionized water.
- [c4] 4 The method of claim 1, wherein the anisotropic etching process comprises a plasma etching process.
- [c5] 5. The method of claim 4, wherein the plasma etching process is performed by using chlorine/hydrogen bromide/oxygen as a reaction gas.
- [c6] 6 The method of claim 1, wherein the concave surface of the remaining conductive layer is higher than a surface of the pad layer.
- [c7] 7 The method of claim 1, wherein the substrate comprises a silicon substrate.
- [c8] 8 The method of claim 1, wherein the conductive layer comprises a polysilicon layer.
- [c9] 9 The method of claim 1, wherein the mask layer comprises a silicon nitride layer.
- [c10] 10 The method of claim 1, wherein the pad layer comprises a silicon oxide layer.

